A CMOS Differential Voltage-to-Frequency Converter with Temperature Drift Compensation

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Abstract

This paper presents a new CMOS differential voltage-to-frequency converter (VFC) which targets front-end sensor interfacing in wireless sensor network applications. The proposed VFC, designed in a low-cost 0.35 μm CMOS technology supplied at 3 V, achieves high performances: power consumption below 0.3 mW, 0 - 2V differential input range operation and nonlinearity error less than 0.3 %. Thanks to the introduction of a very simple control circuit, linearity is preserved over variations of temperature: the error is less than 2.3 % over all the frequency range for a temperature range from -40ºC to +120ºC.

Keywords: Low-voltage low-power CMOS design, smart sensors, quasi-digital sensors, voltage-to-frequency converter, WSN.

1 Introduction

Wireless sensor networks (WSNs) constitute the new paradigm of miniaturization and ubiquity of computing devices, exhibiting an ever-increasing broad variety of distributed wireless sensing applications including medical, home security, military, environmental monitoring, chemical/biological detection or precision agriculture (B. Krishnamachari, 2005; N. P. Mahalik, 2007).

Typically, a wireless sensor node consists of sensing, computing, communication, actuation, and power components. Within the field of sensing, today’s market is advanced towards the so called smart sensors, i. e., integrated intelligent sensor systems that contain on a single chip microsensors (or microsensor arrays) next to all the related sensor electronics for the signal conditioning, processing and conversion necessary to interface the microcontroller (Meijer , 2008).

Inherent to the extensive use of microcontroller based measurement systems, voltage to frequency conversion has risen as a highly suitable alternative to the standard analogue-to-digital (A/D) conversion (Figure 1a) to digitize the conditioned sensor signal: a frequency output signal can be directly interfaced to the microcontroller, which performs the A/D conversion using its internal timers, as shown in Figure 1b.
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Figure 1: Smart sensor: (a) conventional set-up and (b) set-up using VF converter with A/D conversion implemented in the microcontroller.

This simple approach offers several advantages, the most noteworthy being high noise immunity, ease of transmission, wide dynamic range and high accuracy of the frequency to code conversion, existing a speed/accuracy trade-off which can be overcome by using efficient frequency counting techniques (Meijer, 2008).

Various integrated bipolar and CMOS voltage-to-frequency converters (VFC) have been reported up to date. Some integrated bipolar (Cai, 1994) and most of recently reported CMOS (Wang, 2007) VFCs are based on an input voltage-to-current converter followed by a current to frequency converter. All these VFC circuits operate in single-input configuration. Nevertheless, differential signal processing presents one evident and important advantage from the non–differential one: in non–differential processing, both signal and noise are processed, while in differential signal processing, as the difference between two signals is processed, the common-mode noise distortion component is ideally removed. On the other hand, to optimize the size and reduce the cost of the system, CMOS is the preferential technology choice.

This paper presents a CMOS differential voltage-to-frequency converter, which linearly converts the differential sensed voltage into frequency while, thanks to a simple control circuit, high immunity to variation in temperature and voltage supply is attained. The paper is organized as follows. Section II explains the principle of the proposed voltage to frequency converter, including the temperature control circuit. Section 3 reports the results obtained for a 3 V – 0.35 μm CMOS implementation. Finally, conclusions are drawn in Section 4.

2 CMOS Voltage-to-Frequency Converter

2.1 Principle of Operation

The basic scheme of the proposed CMOS voltage to frequency converter is shown in Figure 2 (a). It consists of a MOS resistive circuit (MRC) based voltage integrator driven by a classical Schmitt–Trigger comparator.

The MOS resistive circuit (Figure 2(b)) is formed by four PMOS matched transistors operating in triode region. The use of approximate strong-inversion MOS models demonstrate(Czarnul, 1986) that this configuration ideally cancels both even and odd harmonic distortion terms in the
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Figure 2: (a) Block diagram of the proposed voltage to frequency converter and (b) MOS Resistive Circuit structure

differential current $I_1 - I_2$ produced by the two input voltages $V_1$ and $V_2$, given by:

$$I_1 - I_2 = 2K(V_{G1} - V_{G2})(V_1 - V_2)$$

with

$$K = \frac{1}{2} \mu C_{ox} \frac{W}{L}$$

where $\mu$ is the carrier effective mobility in the channel; $C_{ox}$ is the gate oxide capacitance per unit area; $L$ and $W$ are, respectively, the length and width of the MRC transistors and $V_{G1}$, $V_{G2}$ the applied gate voltages.

This cell can be used to implement a MOSFET-C differential integrator, as shown in the general scheme of Figure 2 (a). Applying input signals expressed as $V_1 = V_{cm} + \frac{1}{2} V_{in}$ and $V_2 = V_{cm} - \frac{1}{2} V_{in}$, where $V_{cm}$ is the common-mode voltage and $V_{in}$ is the differential-mode voltage, the generated differential current (1) will be given by

$$I_1 - I_2 = \frac{1}{R} V_{in}$$

with

$$R = \frac{1}{2K(V_{G1} - V_{G2})}$$

where $R$ is the differential resistance of the MRC. Note that only $V_{in}$ is processed, while the input common voltage $V_{cm}$ is rejected.
This differential current $I_1 - I_2$ is used to both charge and discharge the integrating capacitors $C$ through the differential MRC resistance $R$ depending on the sign of the gate control signal $(V_{G1} - V_{G2})$ between the stable low and high limits $V_L, V_H$ of the succeeding Schmitt-Trigger comparator. The inverting $S_{UP}$ and non-inverting $S_{DW}$ outputs of the Schmitt–Trigger, conveniently modulated by the control circuit, determine the $V_{G1} - V_{G2}$ sign. Assuming that $V_{in}$ is positive during all the cycle, when $V_{cap}$ reaches $V_H$, the comparator outputs flip to $(S_{UP} = '1', S_{DW} = '0')$, setting $V_{G1} - V_{G2} > 0$ and thus starting the discharging period.

Next, when $V_{cap}$ downs to $V_L$, the comparator output flips to $(S_{UP} = '0', S_{DW} = '1')$, setting $V_{G1} - V_{G2} < 0$ and the charge period starts.

In this way, a repeated charge and discharge loop is carried out, with a frequency of oscillation $f_O$ given by

$$f_O = \frac{I_1 - I_2}{2 \cdot C(V_H - V_L)} = \frac{V_{in}}{2RC(V_H - V_L)} \quad (5)$$

The control circuit (Figure 3, protected under patent) is a compact structure which has two main purposes: (i) to generate adequate voltage levels for the controlling signals $V_{G1}$ and $V_{G2}$ from digital signals $S_{UP}$ and $S_{DW}$ and (ii) to provide the adequate variation in $V_{G1}$ and $V_{G2}$ voltages to compensate deviations in the output frequency due to thermal effects.

### 2.2 Design Considerations

The VFC of Figure 2 has been designed in a low-cost 0.35 μm CMOS technology, with single 3V supply and $V_{cm} = 2V$.

For the MRC structure, the width of all the PMOS transistors is set to 4 μm, with a length of 20 μm to avoid short channel effects. A difference voltage gate $|V_{G1} - V_{G2}|$ of 0.3 V is applied, so the equivalent resistive value $R$ is approximately 415 kΩ.
A classical two-stage PMOS input operational amplifier (AO) is used, which shows a differential gain $A_d$ of 92 dB and a unity-gain frequency of 132 MHz with 89º phase margin. The integrating capacitors, $C$, are fixed to 10 pF.

The Schmitt-Trigger comparator employed is the classical digital cell Schmitt-Trigger. The width of all the transistors is set to 10 $\mu$m, with a length of 0.35 $\mu$m, so the comparison limits are approximately given by $V_L=0.92$ V and $V_H=1.82$ V and the rise/fall time equals to 0.62/0.23 ns approximately.

In the control circuit, at room temperature, the voltage gates $V_{G1}$ and $V_{G2}$ take values 0 or 0.3 V, so $(V_{G1} - V_{G2})$ varies from -0.3 in the charge period to 0.3 V in the discharge period.

3 Results

The proposed VFC has been designed in the 0.35 $\mu$m CMOS technology from AMS, with single 3 V supply. Main parameters for this technology are summarized in Appendix 1. Simulations have been done through Cadence using Spectre with a BSIM3v3.2 level 53 transistor models.

The output control circuit $V_G$, the output frequency and the capacitor output voltage waveforms in the time domain for 1.25 V input are shown in Figure 4. The corresponding output frequency is 173 kHz.

The ideal $f_{O,\text{id}}$ and simulated $f_{O,\text{sim}}$ output frequencies at room temperature over all the input voltage range from 0.0 to 2.0 V in 0.2 V steps are shown in Figure 5 (a), where the ideal values are those computed from equation (5). The output frequency varies linearly from 0 to 260 kHz given a 0–2 V input, which results in a sensitivity of 130 kHz/V.

The frequency output error, computed as the relative error $(f_{O,\text{sim}} - f_{O,\text{id}})/f_{O,\text{id}}$ in percentage form is depicted in Figure 5 (b). The maximum error obtained is less than 7.0 % over all the range. The obtained linearity error is 0.3 %.

![Figure 4: Time domain waveforms for $V_{in}=1.25$ V: $(V_{G1} - V_{G2})$ (a) and $V_{cap}$ and output frequency (b)](image-url)
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To validate the proposed temperature compensation circuit, the VFC frequency output vs. temperature for 1 V differential input is shown in Figure 6 without and with temperature compensation.

The frequency output error, computed as the relative error \((f_{O,sim} - f_{O,T0})/f_{O,T0}\) where \(f_{O,T0}\) is the value of the frequency output at room temperature and 3 V supply and \(f_{O,sim}\) the output frequency obtained in simulation, is reduced from 30 % to 1.77%.

The VFC frequency output vs. differential voltage input for a temperature range from -40°C to +120°C using the control circuit (with temperature compensation) is shown in Figure 7 (a). The frequency output error is depicted in Figure 7 (b). The maximum error is less than 2.3 % over all the range.

Figure 6: Frequency output vs. Temperature for 1 V Differential input voltage without thermal compensation (-•-) and compensated (-■-)

Figure 5: (a) Simulated frequency output vs. Differential input voltage at room temperature (27°C) and (b) Output VFC frequency error (%)

To validate the proposed temperature compensation circuit, the VFC frequency output vs. temperature for 1 V differential input is shown in Figure 6 without and with temperature compensation.

The frequency output error, computed as the relative error \((f_{O,sim} - f_{O,T0})/f_{O,T0}\) where \(f_{O,T0}\) is the value of the frequency output at room temperature and 3 V supply and \(f_{O,sim}\) the output frequency obtained in simulation, is reduced from 30 % to 1.77%.

The VFC frequency output vs. differential voltage input for a temperature range from -40°C to +120°C using the control circuit (with temperature compensation) is shown in Figure 7 (a). The frequency output error is depicted in Figure 7 (b). The maximum error is less than 2.3 % over all the range.

Figure 6: Frequency output vs. Temperature for 1 V Differential input voltage without thermal compensation (-•-) and compensated (-■-)
Figure 7: (a) Frequency output vs. Differential input voltage for different temperatures and (b) Output VFC frequency error (%)

The main performances of the proposed voltage-to-frequency converter are summarized on Table I, where we also make a comparison between our design and prior VFC design, based on the classical technique of mirrors system and voltage window comparator.

This new design consumes less than 0.3 mW over all the frequency output range and obtains better performance characteristics in terms of voltage input range operation and immunity to thermal variations. In fact, the maximum error figures given the operating condition of a 10 % supply variation and a temperature range from -40 to 120ºC are reduced from 10 to 8.4 %.

The sensitivity can be widening by adjusting the MRC transistor sizes: according to equation (5), the output frequency range can be selected by modifying the value of the differential MRC resistance $R$ while the integrating capacitor $C$ and comparison level ($V_H-V_L$) are kept constant. Hence, to achieve frequency programmability each MOS transistor in the MRC can be replaced by an identical array of MOS transistors with different sizes ($W/L$).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This work</th>
<th>(Wang, 2007)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35 μm CMOS</td>
<td>0.25 μm CMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3.0 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>$\geq 130$ kHz/V</td>
<td>$\geq 58$ MHz/V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>0.0 V – 2.0 V</td>
<td>0.0 V – 0.9 V</td>
</tr>
<tr>
<td>Max. Error (Sensitivity)</td>
<td>7 %</td>
<td>8 %</td>
</tr>
<tr>
<td>Max. Error (Linearity)</td>
<td>0.3 %</td>
<td>----------------</td>
</tr>
<tr>
<td>Max. Error (Temperature)</td>
<td>2.3 %</td>
<td>10 %</td>
</tr>
<tr>
<td>Power consumption</td>
<td>0.273 mW</td>
<td>0.218 mW</td>
</tr>
</tbody>
</table>

Table 1: Summary and comparison of VFC Performances.
Their gate may be controlled by means of a digital word which modifies the equivalent \((W/L)\) and thus the achievable frequency range as follows:

\[
\begin{align*}
 f_{\text{in}} &= \frac{V_{\text{in}}}{2R_c(V_{H} - V_{L})} = \frac{\mu C_{\text{ox}}W_c(V_{G1} - V_{G2})}{2L_c(V_{H} - V_{L})} V_{\text{in}} \\
 &\quad (6)
\end{align*}
\]

Designed for differential input voltages, it is also possible to work with single voltage input with a higher sensitivity and one half of the differential voltage input range.

**4 Conclusions**

A very simple CMOS differential voltage to frequency converter structure has been presented focusing on the present day increasing demand for low-cost, high performance, low-power interface electronics targeting wireless sensor networks applications. Results from a 3 V–0.35 \(\mu\)m CMOS design show a good trade off between sensitivity, linearity and power consumption. In addition, this structure presents high immunity to thermal effects.

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**References**


