A complete low voltage analog lock-in amplifier to recover sensor signals buried in noise for embedded applications

M. Gabal, N. Medrano, B. Calvo, S. Celma, P. A. Martinez

Affiliation: Group of Electronic Design.
Aragon Institute of Engineering Research (I3A).
University of Zaragoza, Maria de Luna 3, 50015, Zaragoza, Spain.
Tel. +34-976761240, Fax +34-976762143, e-mail: mgabal@unizar.es

Abstract

This paper presents a complete low-voltage 3V single supply analog lock-in amplifier (LIA) based on phase sensitive detection technique (PSD) for processing AC sensor signals buried in noise in embedded wireless applications. Reference and bias sensor signals are provided by a quadrature oscillator. Experimental results confirm the capability of the proposed lock-in amplifier to effectively recover information from signal to noise ratios below -32 dB with errors below 9%. This general system is valid to work both for resistive to capacitive sensors. In addition, the system presents three different power modes that permit extending the battery operation lifetime of the system.

Keywords: Lock-in amplifier; phase-shift detector; conditioning electronics; sensor signal conditioning.

1 Introduction

Sensors convert physical phenomena into electrical signals so that they can be processed. In some applications, the sensor output signals can have extremely small amplitude, which can even be smaller than the electrical noise level. In these cases, linear filtering is not a suitable processing method to extract signal information, making necessary the use of special techniques. An interesting possibility is the use of lock-in amplifiers (Meade, 1983; Princeton, 1971; Stanford, 1999), which use the phase-sensitive detection technique (PSD) to single out the data signal at a specific reference frequency. Noise signals at frequencies other than the reference are rejected, do not affecting significantly the results.

Lock-in amplifiers have been used in a broad number of areas including radio astronomy, nuclear magnetic resonance, electron spin resonance, optical interferometer fringe position monitors and control of gas absorption stabilized lasers (Blair, 1975). Current commercial lock-in amplifiers are expensive, large in dimensions, heavy and not suitable for portable applications.

In this work the possibility of exporting this technique to low-voltage single-supply systems is proposed. We present a signal conditioning architecture for single-supply embedded applications in extremely noisy environments which can be applied to low-power low-voltage applications, as 3 V battery operated sensor nodes from a Wireless Sensor Network (WSN) system.
A complete low voltage analog lock-in amplifier

This paper is organized as follows: Section 2.1 presents a brief introduction to classical lock-in amplifiers, showing their limitations for low-power single-supply applications; in Section 2.2, the main blocks of the designed analog lock-in amplifier are shown; Section 2.3 will show the experimental characterization setup of the proposed architecture using commercial components; in Section 3 we present some experimental results achieved using the proposed system applied to signals with different noise levels.

2 Lock-in Amplifiers

2.1 Principle of Operation

Lock-in amplifiers are used to detect and measure low-level AC signals. Accurate measurements may be made even when the signal carrying the information is affected by high noise levels. For this, lock-in amplifiers use a technique known as phase-sensitive detection to obtain the absolute mean value of the data signal at a specific reference frequency. Noise signals, at frequencies other than the reference frequency, are rejected and do not affect the measurement.

This measurement technique requires a frequency reference. Typically, a device is excited by a signal with a fixed frequency, and the lock-in detects its response. The exciting signal is alternatively multiplied by 1 and -1, according to the value of a control signal (Figure 1). By properly synchronizing the data and control signals, it is possible to measure the absolute mean value of the data signal, rejecting the noise.

Phase-sensitive detection can be performed in two different ways: analogue and digital PSD. Depending on the processing system characteristics, the PSD method is performed on the digitized signal, using digital signal processing techniques. This option is suitable when the processing electronics includes a processor with enough computing power to perform the mathematical operations needed. However, for low-power portable embedded applications, as wireless sensor networks, which include low-cost microcontrollers with limited computing power, the use of analogue lock-in amplifiers is the best solution.

Currently, analogue lock-in amplifiers are designed using dual power supply (Gnudi, Colalongo, and Baccarani, 1999; D’Amico et al., 2009). In this way, sensor and control signals present both positive and negative half-periods. This characteristic is exploited in the system

Figure 1: Digitally switched analog mixer, and the low-pass filter that provides the data signal average value.
operation, synchronously rectifying the input signal (Figure 1), and cancelling the noise effects. However, dual power supply limits significantly their application in portable systems, as battery-operated wireless sensing networks (Bayo et al., 2010). In these systems, whose energy is usually provided by two 1.5 V batteries, it is necessary to design the processing elements working in single supply operation.

2.2 Proposed Lock-in Amplifier Main Blocks

Figure 2 shows the proposed lock-in amplifier (LIA) block scheme. It has been designed as a full system to recover information from signals provided by sensors in noisy environments. It has been designed to be a part of the sensor signal processing system of a node in a wireless sensor network. The system operates at a 3 V single supply and consists of a quadrature oscillator that feeds the sensor and drives two parallel PSD branches eliminating the system phase dependence (Stanford, 1999), thus enabling its use for both resistive and capacitive sensors.

Each of the PSD lines consists of a comparator, a mixer and a low-pass filter. The input signal is provided by the sensor whose signal is processed. The comparators provide two reference square waves at the same frequency \( f_o \) than the sensor output signal and a phase shift of 90 degrees between them. Using these signals to control the mixer operation, the sensor output will be selectively rectified. Finally, the resulting signals are low-pass filtered in the last stage, obtaining their average value. By properly combining the information provided by both processing lines, it is possible to recover the sensor signal, independently of the noise present in the system.

2.3 Experimental Setup

In this section an experimental characterization of the proposed structure is presented. Using commercial ICs, we assembled the circuit of the block diagram (Figure 2). To simulate the behaviour of the sensor in a low signal to noise ratio (SNR) environment we make use of a data acquisition (DAQ) board USB6212 (National Instruments, 2009), which provides 16 analog input (AI) and two analog output (AO) channels, two counters and 32 bidirectional static DIO lines. The DAQ board has a sampling rate up to 250,000 samples/s.
Figure 3: Noisy sensor signal simulation circuit.

Figure 3 shows the setup designed to simulate the behaviour of a sensor in a controllable noise environment. In this case operational amplifiers are split supplied (-3.5V +3.5V), as for characterizing the system it is not necessary to satisfy the constraints of 3 V single supply. Ideal sensor signal ($V_1$) is provided by one of the outputs of the quadrature oscillator. The stage a) removes the DC level of the signal with a capacitor $C_1=1 \mu F$. The next stage b) is an inverting amplifier with a gain <1 that reduces the signal amplitude, thus providing a signal $V'$ which represents the sensor output free of noise and DC levels. This signal is acquired by the DAQ board to evaluate the operation performance of the designed LIA. Stage c) is a three input inverting adder that creates the simulated full sensor signal: the input $V_C$ is a -1.5 V constant voltage that restores the original DC level, while the white noise of controllable amplitude ($V_N$) is provided by the DAQ, thus simulating the noisy sensor signal ($V'+V_N+ V_C$) that is processed by the proposed system.

### 2.3.1 Quadrature Oscillator

The feed and control of the system is given for a variable frequency quadrature oscillator shown in Figure 4. It consists of two integrators and an inverter amplifier. His frequency and the oscillation condition are controlled for resistive elements:

$$f_o^2 = \frac{1}{C^2 R_A R_B} \quad \text{if} \quad R_A = R_B \quad (1)$$

Figure 4: Quadrature Oscillator: $V_1$ and $V_2$ are the system 90 degrees of phase shift outputs.
A complete low voltage analog lock-in amplifier

The oscillator has been built using rail-to-rail MAX4250 OpAmps (Maxim, 2005) at 3 V supply. The oscillator provides two 140 Hz sinusoidal signals with 1.5 V of amplitude and 1.5 V DC level, which centres the signal in the bias voltage range.

On the other hand, the outputs of the quadrature oscillator are converted to two square waves with 90 degrees of phase shift by means of two comparators (Figure 2) built with MAX4250 rail-to-rail single supply OpAmps (Maxim, 2005). These signals drive the corresponding mixers.

2.3.2 Single Supply Mixer

The design of the mixer, the fundamental block of the lock-in amplifier, has to be done considering its operation in single supply mode.

The proposed structure, shown in Figure 5b, consists of two CMOS ADG719 switches from Analog Devices (Analog Devices, 2002), switched according to the value of the reference signal: the inputs of the INA327 precision amplifier (Texas Instruments, 2008) are selected so that it acts like a mixer with unity gain. The operation of the mixer is given by:

\[
V_o = \begin{cases} 
(V_{in} - 0) & \text{if } V_{in} > 1.5V \\
(3 - V_{in}) & \text{if } V_{in} < 1.5V 
\end{cases}
\] (2)

Where \(V_o\) is the output of the system and \(V_{in}\) is the signal to be processed. The resulting output voltage of the mixer, if \(V_{in}\) and REF have the same phase, is shown in Figure 5c.

The rectified signal is fed to a lowpass filter with a corner frequency lower than \(f_o\) in order to extract its DC level (\(V_{DC}\)). In this implementation we have selected an RC circuit with a cut-off frequency \(f_c = 1.59\) Hz.

The resulting DC signals \(V_{01}\) and \(V_{02}\) (Figure 2) can be processed by a microcontroller, obtaining the noise-free amplitude of the signal \(V_S\) provided by the sensor according to:

\[
A = \frac{\pi}{2} \sqrt{(V_{01} - 1.5)^2 + (V_{02} - 1.5)^2}
\] (3)

Where \(2/\pi\) is the mean absolute value of the sine function.

Figure 5: (a) Input signal to the mixer; (b) Signal mixer; (c) Rectified output signal
A complete low voltage analog lock-in amplifier

Figure 6: Input signal to the LIA in blue (top) and the mixer output signals in pink (middle) and green (bottom) for (a) 0 V of noise contamination (SNR=∞), and (b) SNR=-17 dB (noise amplitude is 7 times higher than data signal).

3 Results

The performance of the designed analog lock-in system to recovering information from noisy signals has been evaluated using a sinusoidal signal with a controllable SNR provided by the sensor noise simulation circuit.

Figure 6 shows two cases with different SNR values: a signal free of noise (V’=100 mV, V_N=0 V) (Figure 6a, top), and a signal with noise amplitude 7 times higher than the signal (V’=100 mV, V_N=700 mV) (Figure 6b, top). In both cases, the sensor signal is show in blue. Due to its characteristics, the signal in Figure 6a can be processed by means of conventional techniques, while the processing of the signal shown in Figure 6b requires special techniques. The proposed system is capable to extract information from signals with this contamination level and even greater.

The designed LIA system ability to recover information from signals buried in noise has been evaluated. Figure 7 shows the error achieved in the recovery of the noise-free amplitude of the sensor signal for different noise levels, using a 28 mV signal amplitude with 11 different noise amplitude values. As we can see, measurement errors are below 9% for SNR up to -32 dB (noise levels 40 times higher than the signal amplitude).

Wireless sensor network applications are limited by battery operation life. Thus, in sensor conditioning circuits designed for these applications power consumption is an important restriction. In order to extend battery operation, the proposed system allows three power modes: switch off, sleep and awake. In the first mode the LIA is disconnected from the power source, avoiding energy consumption. In sleep mode, all components are switched on but the precision amplifiers of the signal mixers (the most power consuming elements in the system), that are in shutdown mode. In this case, power consumption is lower than 1 mW. Finally, in full operation mode the average consumption is 20 mW.
A complete low voltage analog lock-in amplifier

Figure 7: Errors in the estimation of the signal amplitude for 11 different SNR. Error remains below 9% for noise levels 40 times higher than data signals

4 Conclusions

This paper proposes the architecture of a processing system for wireless embedded applications in low SNR environments. This system is based on a lock-in amplifier based on phase-sensitive detection technique. Restrictions due to single supply operation have required the redesign of the signal mixer, responsible to reject the noise signal.

In addition, the need of low form factor and power consumption related to wireless sensor network applications makes necessary the use of low-power low-voltage electronic components and a precise power management to extend the battery operation. Using commercial components, the analog lock-in amplifier has been designed according to those restrictions, and can be applied to active sensors in embedded wireless applications. Figure 8 shows a photograph of the tested prototype made with SMD components.

Figure 8: Compact lock-in amplifier prototype made with SMD components
A complete low voltage analog lock-in amplifier

Experimental measurements have confirmed the capability of the proposed lock-in system to recover signals with a low SNR level (< -32 dB) with errors below 9%. For this, the amplifiers included in the signal mixers must present a true input rail-to-rail characteristic, which currently penalizes the power consumption. Currently we are working to replace those elements (the instrumentation amplifiers in the signal mixers), for low-power devices that will provide similar results.

5 Acknowledgments

This work was supported by the I3A fellowship program, MICINN (RYC-2008-03185, PET2007-00336, PET2008-0021 and TEC2009-09175), DGA-La Caixa (GA-LC-039/2008, GA-LC-033/2009) and DGA (PI 113/09).

References


Analog Devices (2002). *CMOS 1.8 V to 5.5 V, 2.5 Ohm 2:1 Mux/SPDT Switch in SOT-23*. Analog Devices.